IN THE CLAIMS

Please amend the claims as follows:

Claims 1-4 (Cancelled).

Claim 5 (Original): A manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film and a second gate insulating film on said semiconductor substrate via a first gate insulating film;

etching said second gate insulating film and the underlying first gate electrode material film to make slits that separate said first gate electrode material film above said element isolation/insulation films;

forming an insulating film on side surfaces of said first gate electrode material film, and thereafter stacking a second gate electrode material film;

sequentially etching said second gate electrode material film, said second gate insulating film and said first gate electrode material film to pattern said first gate electrode film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self alignment with said control gates.

Claim 6 (Original): The manufacturing of a nonvolatile semiconductor memory device according to claim 5 wherein said first gate electrode material film is a multi-layered film including a first conductive film stacked before formation of said element isolation/insulation films and a second conductive film stacked after formation of said element isolation/insulation film.

Claim 7 (Currently Amended): The manufacturing of a nonvolatile semiconductor memory device according to ~~one of claims~~ claim 5 wherein said element isolation/insulation films are buried in grooves formed into said semiconductor substrate.

Claim 8 (Original): The manufacturing of a nonvolatile semiconductor memory device according to claim 5 wherein said second gate insulating film is a multi-layered film including silicon oxide film / silicon nitride film / silicon oxide film.

Claim 9 (Currently Amended): The manufacturing of a nonvolatile semiconductor memory device according to ~~one of claims~~ claim 6 wherein said element isolation/insulation films are buried in grooves formed into said semiconductor substrate.

Claim 10 (Original): The manufacturing of a nonvolatile semiconductor memory device according to claim 6 wherein said second gate insulating film is a multi-layered film including silicon oxide film / silicon nitride film / silicon oxide film.

Claim 11 (Original): The manufacturing of a nonvolatile semiconductor memory device according to claim 7 wherein said second gate insulating film is a multi-layered film including silicon oxide film / silicon nitride film / silicon oxide film.

Claim 12 (Original): A manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film and a second gate insulating film on said semiconductor substrate via a first gate insulating film;

etching said second gate insulating film and the underlying first gate electrode material film to make slits that separate said first gate electrode material film above said element isolation/insulation films;

sequentially stacking a third gate insulating film and a second gate electrode material film;

sequentially etching said second gate electrode material film, said third and second gate insulating films, and said first gate electrode material film to pattern said first gate electrode material film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self-alignment with said control gates.

Claim 13 (Original): A manufacturing method of a nonvolatile semiconductor memory device, comprising the steps of:

making element isolation/insulation films that partition element-forming regions in a semiconductor substrate;

stacking a first gate electrode material film on said semiconductor substrate via a first gate insulating film;

etching said first gate electrode material film to make slits that separate said first gate electrode material film on said element isolation/insulation films;

etching surfaces of said element isolation/insulation films exposed to said slits to make recesses;

stacking a second gate electrode material film on said first gate electrode material film and said element isolation/insulation films via said first gate insulating film;

sequentially etching said second gate electrode material film, said gate insulating film and said first gate electrode material film to pattern said first gate electrode material film into floating gates and said second gate electrode material film into control gates; and

making source and drain diffusion layers in self-alignment with said control gates.